

PAIDC

QUERY CONTROL FORM		RTIS USE ONLY	
Application No. <u>101620,208</u>	Prepared by <u>NH</u>	Tracking Number <u>05894361</u>	
Examiner-GAU <u>Audung-2818</u>	Date <u>2-17-4</u>	Week Date <u>01/26/04</u>	
	No. of queries <u>1</u>	<u>IFW</u>	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. <u>PTO-1449</u>
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION	MESSAGE
a. Page Missing	<p><u>PTO-1449: Please either initial or line through citations. Copy provided for reference.</u></p>
b. Text Continuity	
c. Holes through Data	
d. Other Missing Text	
e. Illegible Text	
f. Duplicate Text	
g. Brief Description	
h. Sequence Listing	
i. Appendix	
j. Amendments	
k. Other	
<b>CLAIMS</b>	
a. Claim(s) Missing	
b. Improper Dependency	
c. Duplicate Numbers	
d. Incorrect Numbering	
e. Index Disagrees	
f. Punctuation	
g. Amendments	
h. Bracketing	
i. Missing Text	
j. Duplicate Text	
k. Other	
	<p><b>RESPONSE</b> <u>Doze</u></p> <p><u>Thank you</u></p> <p><u>Jeff</u></p>
	<p>initials <u>NH</u></p>
	<p>initials <u>P</u></p>

**UNITED STATES DEPARTMENT OF COMMERCE****U.S. Patent and Trademark Office**

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
---------------------------------	-------------	---	---------------------

EXAMINER
----------

ART UNIT	PAPER
----------	-------

031504

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents


Attached is the PTO-1449 that initial to consider the cited references that missing from previous mailed.

Gene N Auduong  
Primary Examiner  
Art Unit: 2818



# Electronic Information Disclosure Statement











## System and Method to Screen Defect Related Reliability Failures in CMOS SRMAS

Application:   
10/020208  
Confirmation: 7966  
Applicant(s): Surya Bhattacharya  
Docket Number: 1875.0330001  
Group Art Unit: 2818  
Examiner:  
search string: (5745415 or 5661729 or 6154403 or 6115304 or 6081464 or 6038189).on



RECEIVED  
APR 10 2003  
TC 800 MAIL ROOM

### US Patent Documents


Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Citation No.	Patent Number	Date	Bar Code	Patentee	Class	Subclass
	P01	5745415	1998-04-28		Marr	365	201
	P02	5661729	1997-08-26		Miyazaki et al.	714	719
	P03	6154403	2000-11-28		Tanzawa et al.	365	203
	P04	6115304	2000-09-05		Suga	365	201
	P05	6081464	2000-06-		Marr	365	201

10/020,208

			27		
	P06	6038181	2000-03-14		Braceras et al. 365/201

### Signature

Examiner Name	Date
	5/03